THE CLAIMS

Claims 1-40 are pending in the instant application. Independent claims 1, 21 and 32 have been amended. Claims 2-20, 22-31 and 33-40 depend from independent claims 1, 21 and 32, respectively.

The Applicant requests reconsideration of the claims in view of the following amendments reflected in the listing of claims.

Listing of claims:

1. (Currently Amended) A method for reducing phase noise, comprising:

generating a signal at a particular frequency, the signal being associated with a harmonic frequency signal disposed at a harmonic frequency;

selecting frequency content disposed in a region around the harmonic frequency; and

~~selectively~~ attenuating said selected frequency content disposed in [[a]]said region around the harmonic frequency.

2. (Previously Presented) The method of claim 1, comprising:

associating the signal with a second harmonic frequency signal disposed at a second harmonic frequency; and

selectively attenuating frequency content disposed in a second region around the second harmonic frequency.

3. (Previously Presented) The method of claim 1, comprising:

applying at least one non-linear operation to the signal; and

transmitting the applied signal.

4. (Original) The method of claim 3, wherein applying at least one non-linear operation to the signal comprises dividing the signal.

5. (Original) The method of claim 3, wherein applying at least one non-linear operation to the signal comprises mixing the signal with a reference signal.

6. (Original) The method of claim 3, wherein applying at least one non-linear operation to the signal comprises amplifying the signal.

7. (Original) The method of claim 1, wherein the signal is generated by at least one of a fixed frequency oscillator, a voltage controlled oscillator, and a current controlled oscillator.

8. (Original) The method of claim 1, wherein the frequency content is selectively attenuated by at least one attenuating circuit.

9. (Original) The method of claim 8, wherein the at least one attenuating circuit comprises at least one of an integrated component and a discrete component.

10. (Original) The method of claim 8, wherein the at least one attenuating circuit comprises at least one harmonic trap.

11. (Previously Presented) The method of claim 1, comprising:

buffering the signal prior to selectively attenuating the frequency content.

12. (Original) The method of claim 11, wherein the buffering is performed by a buffer.

13. (Original) The method of claim 12, wherein the selective attenuating of the frequency content is performed within the buffer.

14. (Original) The method of claim 1, wherein the signal comprises a differential signal.

15. (Original) The method of claim 1, wherein the signal comprises a quadrature signal.

16. (Original) The method of claim 1, wherein the selective attenuating comprises canceling frequency content disposed in the region around the harmonic frequency.

17. (Original) The method of claim 16, wherein the canceling frequency content disposed in the region around the harmonic frequency comprises canceling frequency content disposed only at the harmonic frequency.

18. (Original) The method of claim 1, wherein the selective attenuating comprises notching frequency content disposed in the region around the harmonic frequency.

19. (Original) The method of claim 18, wherein the notching frequency content comprises notching frequency content disposed only at the harmonic frequency.

20. (Original) The method of claim 1, wherein the selective attenuating comprises bandstopping frequency content disposed in the region around the harmonic frequency.

21. (Currently Amended) A circuit for reducing phase noise, comprising:

a signal generator that generates a signal at a particular frequency, the signal being associated with a harmonic frequency signal disposed at a harmonic frequency; and

an attenuating circuit that selects frequency content disposed in a region around the harmonic frequency and ~~selectively~~ attenuates said selected frequency content disposed in [[a]]said region around the harmonic frequency.

22. (Previously Presented) The circuit of claim 21, comprising:

a buffer for buffering the signal, the buffer being coupled to the signal generator.

23. (Original) The circuit of claim 22, wherein the attenuating circuit is part of the buffer.

24. (Previously Presented) The circuit of claim 21, comprising:

a non-linear operation circuit that applies at least one non-linear operation to the signal to obtain an outgoing signal; and

a transmitting circuit for transmitting the outgoing signal.

25. (Original) The circuit of claim 24, wherein the transmitting circuit comprises an antenna.

26. (Original) The circuit of claim 24, wherein the non-linear operation circuit comprises a divider that divides the signal.

27. (Original) The circuit of claim 24, wherein the non-linear operation circuit comprises a mixer that mixes the signal with a reference signal.

28. (Original) The circuit of claim 24, wherein the non-linear operation circuit comprises an amplifier that amplifies the signal.

29. (Original) The circuit of claim 21, wherein the signal generator comprises at least one of a fixed frequency oscillator, a voltage controlled oscillator, and a current controlled oscillator.

30. (Original) The circuit of claim 21, wherein the attenuating circuit comprises at least one of an integrated component and a discrete component.

31. (Original) The circuit of claim 30, wherein the attenuating circuit comprises at least one harmonic trap.

32. (Currently Amended) A system for reducing phase noise, comprising:

a signal generator that generates a signal at a particular frequency, the signal being associated with a harmonic frequency signal disposed at a harmonic frequency; and

a buffer that buffers the signal, the buffer adapted to select frequency content disposed in a region around the harmonic frequency and ~~selectively~~ attenuate said selected frequency content disposed in [[a]]said region around the harmonic frequency.

33. (Original) The system of claim 32, wherein the signal comprises a differential signal.

34. (Original) The system of claim 32, wherein the signal comprises a quadrature signal.

35. (Original) The system of claim 32, wherein the signal generator comprises a differential signal generator.

36. (Original) The system of claim 35, wherein the buffer comprises a differential pair of transistors, the differential pair of transistors being adapted to receive the signal.

37. (Original) The system of claim 32, wherein the buffer comprises a harmonic trap, the harmonic trap being adapted to attenuate the frequency content disposed in the region around the harmonic frequency.

38. (Original) The system of claim 37, wherein the harmonic trap is disposed across a differential output of the buffer.

39. (Original) The system of claim 32, wherein the buffer is adapted to band stop the frequency content disposed in the region around the harmonic frequency.

40. (Original) The system of claim 32, wherein the buffer is adapted to notch the frequency content disposed only at approximately the harmonic frequency.